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Highly Aligned Scalable Platinum-Decorated Single-Wall Carbon Nanotube Arrays for Nanoscale Electrical Interconnects

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ABSTRACT We present the fabrication and characterization of nanoscale electrical interconnect test structures constructed from aligned single-wall carbon nanotubes using a template-based fluidic assembly process. This CMOS-friendly process enables the formation of highly aligned parallel nanotube interconnect structures on SiO_2/Si substrates of widths and lengths that are limited only by lithographical limits and, hence, can be easily integrated onto existing Si-based platforms. These structures can withstand current densities of $\sim 10^7$ A · cm^{-2}, comparable or better than copper at similar dimensions. Both the nanotube alignment and failure current density improve with decreasing structure width. In addition, we present a novel Pt nanocluster decoration method that drastically decreases the resistivity of the test structures. *Ab initio* density functional theory calculations indicate that the increase in conductivity of the nanotubes is caused by an increase in conduction channels close to their Fermi levels due to the platinum nanocluster decoration, with a possible conversion of the semiconducting single-wall carbon nanotubes into metallic ones. These results reflect a huge step toward the proposed replacement of copper-based interconnects with carbon nanotubes at gigascale integration levels.

KEYWORDS: carbon nanotubes · fluidic assembly · nanoscale interconnects · Pt decoration · SWNT metallization

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As elements of integrated circuits downsize toward a few nanometers, existing interconnect technology faces a tremendous bottleneck due to the electromigration failure of copper (Cu) lines.[1−3] In addition, as the lateral dimension of interconnects approaches the mean free path of Cu ($\sim$40 nm at room temperature), the impact of grain boundary scattering, surface scattering, and the presence of a high-resistivity material as a diffusive barrier layer causes a rapid increase in their overall resistivity. In this context, carbon nanotubes (CNTs) have been envisioned as a possible replacement for copper electrical interconnects for future gigascale integration considering their immense individual failure current densities ($>10^9$ A · cm^{-2}).[4−8] Especially at the nanoscale, highly aligned parallel nanotube architectures comprising all-metallic single-walled carbon nanotubes (SWNTs) are expected to outperform copper in terms of failure current density, power dissipation, and on-chip signal transfer delays.[9−13] However, to fabricate such highly aligned SWNT-based interconnects in an integrated device, a CMOS-friendly scalable manufacturing process that can controllably place aligned SWNTs in desired locations, orientations, and dimensions is extremely crucial. In addition, since naturally grown SWNTs comprise a mixture of metallic and semiconducting nanotubes, there is an imminent need to develop a process that will convert semiconducting nanotubes into metallic ones within such architectures. Therefore, a single-step, simple, and CMOS-compatible method that can simultaneously convert semiconducting SWNTs into metallic ones, and also possibly increase the conductance of existing metallic SWNTs, is highly desirable. Addressing these technological challenges is essential before carbon nanotubes can be realistically implemented as future interconnects.

Recently, we have demonstrated a novel template-based fluidic assembly process for fabricating highly organized SWNT lateral network architectures at wafer scales.[14,15] We have also shown that the conductance of individual multi-wall carbon nanotubes (MWNTs) can be improved significantly by decorating its surface with platinum (Pt) nanoclusters.[16] Field theoretical analysis of the temperature dependence of conductance of these nanotubes confirmed that this is caused by the increase

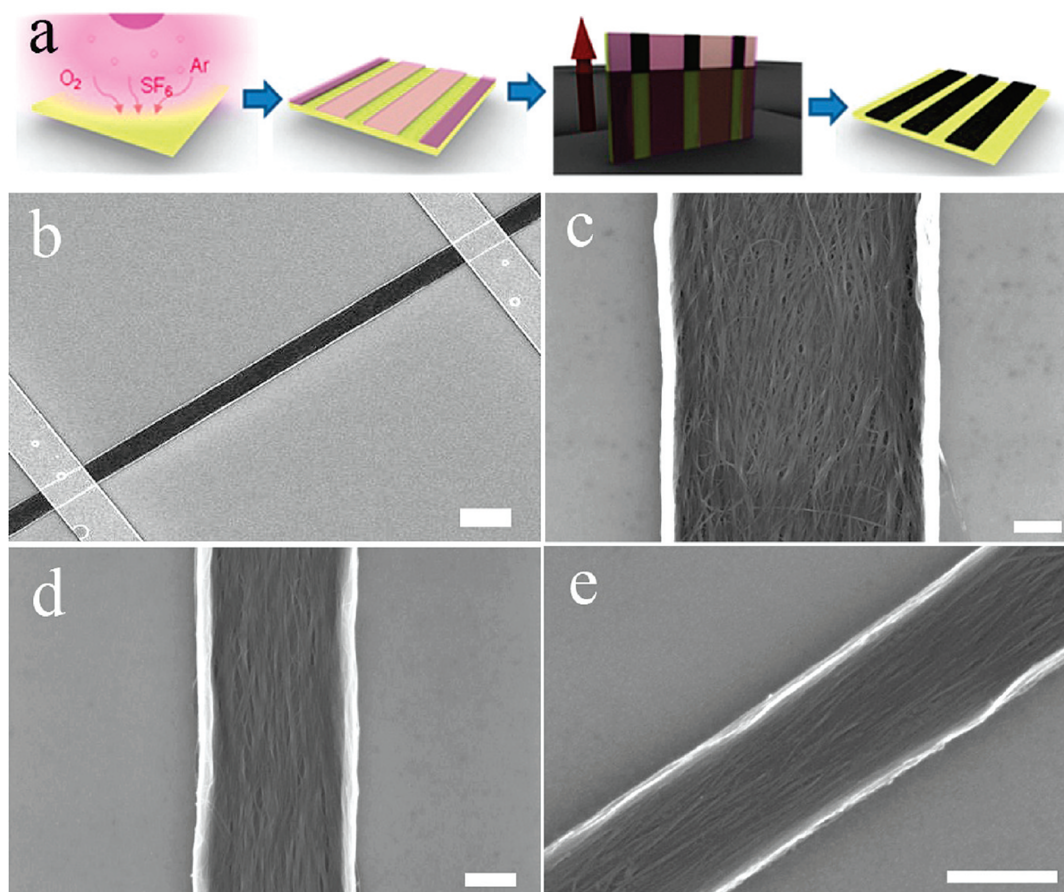

Figure 1. Schematic and SEM images showing super-aligned SWNT interconnect test structures. (a) Schematic showing template-based fluidic assembly of high density and highly aligned SWNT architectures. (b) SEM image of typical SWNT lateral structures with two-probe contact pads. Scale bar = 2 μm. (c−e) High-magnification SEM images showing the degree of alignment of the SWNTs within channel widths of ~1000, ~500, and ~200 nm, respectively. Scale bars = 200 nm.

in the number of conductance channels of the nanotubes. *Ab initio* density functional theory (DFT) calculations indicated that charge transfer from decorated Pt nanoclusters on nanotubes can increase the number of bands near the Fermi level of the nanotubes and increase their density of states (DoS).

In this paper, we combine these ideas to develop highly organized aligned arrays/channels of Pt-decorated SWNT interconnect test structures, with vastly improved performance over pristine SWNT architectures. In general, we find that the nanotube alignment improves noticeably with decreasing lateral channel widths, with the best alignment obtained for widths close to 200 nm. Significantly robust against the lithographic and electrodeposition steps, these interconnect test structures were capable of withstanding current densities up to $\sim 10^7$ A · cm^{-2}. Upon platinum decoration, the average electrical resistivity of these SWNT interconnect test structures decreased by 45%, with a 52% drop for the narrowest channels. Our DFT calculations also show that Pt nanoclusters can convert semiconducting SWNTs into metallic ones and improve the conductance of metallic nanotubes, as well. In more than 25% of the tested structures, the resistance of the Pt-decorated structures fell to 1/3 of its pristine value, indicating that most of the semiconducting nanotubes between the Ti/Au-contacted SWNT arrays have converted to metallic ones. In a few cases, this value fell below 1/3, indicating that the conductance of the metallic nanotubes has gone up, as well. These completely CMOS-compatible and scalable process steps together reflect a huge step toward integration of carbon nanotubes into existing interconnect technologies.

RESULTS AND DISCUSSION

Figure 1 shows representative scanning electron microscopy (SEM) images of our aligned SWNT lateral architectures fabricated on SiO_2/Si substrates using our template-guided fluidic assembly process. Figure 1a schematically explains the basic steps of building organized SWNT lateral architectures. First, a plasma treatment is used to enhance the hydrophilic nature of the SiO_2 surface. Second, 600 nm thick PMMA photoresist patterns are constructed using electron-beam lithography (EBL) to build nanoscale channels which form templates for building the interconnect architectures. Next, these templated substrates are dip-coated in a SWNT−DI water solution at a constant pulling rate of 0.5 mm · min^{-1}, which resulted in stable and densely aligned SWNT lateral network architectures having well-

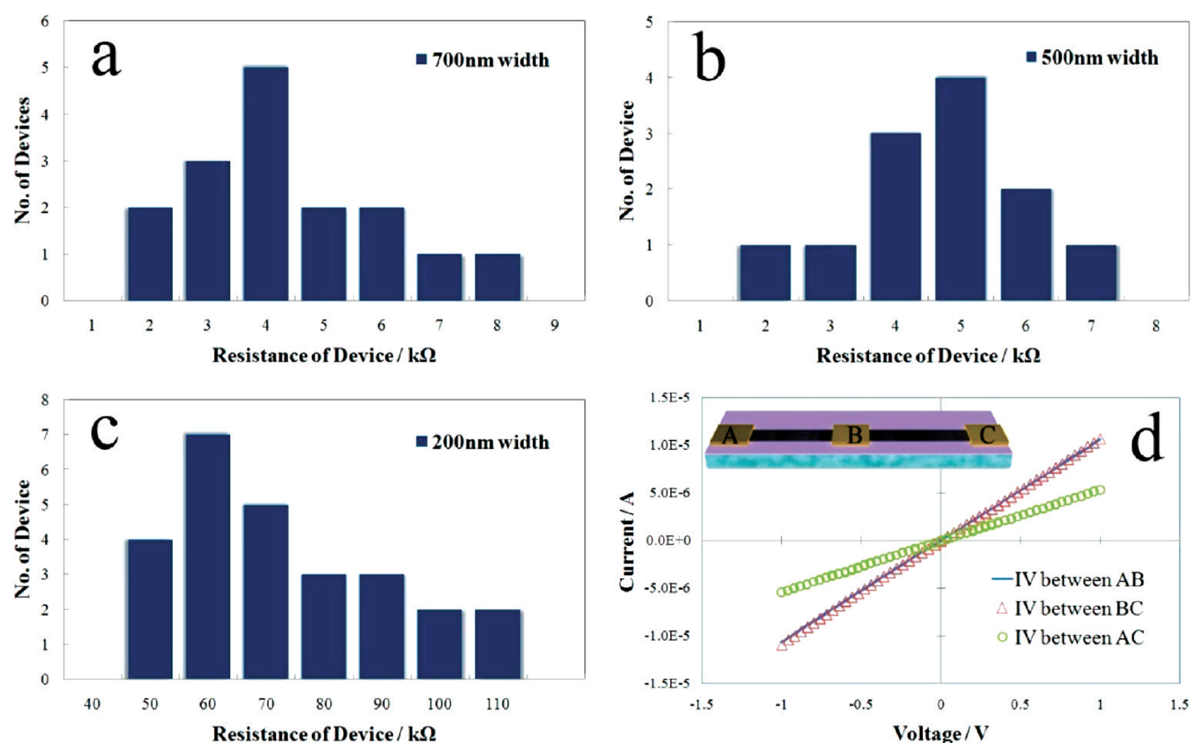

Figure 2. Electrical characterization of aligned SWNT interconnect test structures. (a−c) Resistance histograms of pristine devices. The values were distributed mainly around 4, 5, and 60 kΩ for channel widths of 700, 500, and 200 nm, respectively. (d) Current−voltage ($I-V$) curves between different contact pads A, B, and C separated by a distance of 10 μm between them (as shown in the inset schematic) for calculation of contact resistances (see text).

defined shapes at nanoscale and were defined by the geometry of PMMA patterns on the substrate. We used 0.23 wt % SWNT−DI water solution (obtained from Brewer Science Inc.) with the mean length of 610 nm and mean diameter of 1.9 nm. Finally, the photoresist is removed to obtain well-organized and aligned SWNT lateral networks. Figure 1b is an SEM image of a typical SWNT lateral structure attached on top with two contact pads of Ti/Au, fabricated using a standard EBL process. Panels c−e in Figure 1 are higher magnification SEM images showing the relative alignments of lateral SWNTs along the channels with approximate widths of 1000, 500, and 200 nm, respectively. An important outcome of our SWNT assembly technique is that the degree of alignment of SWNT structures tends to increase with lower channel widths. The details of Raman spectroscopy for the characterization of their alignment are available in the Supporting Information. We believe that the increasing alignment occurs during the dip-coating process due to the increasing confinement of the PMMA trench geometry with decreasing channel widths.

Two-terminal current−voltage ($I-V$) characteristic and resistance R (from the slope of the $I-V$ near V = 0) was measured in all of the test structures before decoration with Pt nanoclusters. A number of test structures (having 25 μm length between two contact pads) of representative channel widths (700, 500, and 200 nm) were characterized this way. Figure 2a−c shows the resistance histograms of the test structures of different channel widths. The resistances of the channels were mainly distributed around 4, 5, and 60 kΩ for channel widths of 700, 500, and 200 nm, respectively, indicating that as the channel width narrows its resistance increases. We observed that test structures with a width of ~200 nm have much higher resistance values compared to the wider channels. Average resistivities calculated for each channel width (see Figure 5d) show an increasing trend when the channel width is decreased, indicating increasing semiconducting behavior as the channel width narrows. Similar observations have been experimentally reported for random SWNT mats with decreasing height.[17] Since we do not yet have a clear understanding of the self-alignment mechanism of SWNTs during the assembly process, especially the degree of alignment with different channel widths, at this stage, we cannot explain this related electronic property change. However, on the basis of previous studies of percolation theory of SWNT networks,[18,19] we feel that the alignment of SWNTs in narrower channels statistically reduces the formation of metallic conduction paths between the two contacts, resulting in a dominant semiconducting property of the arrays.

To estimate the contact resistance for a given test structure, three contact pads (A, B, and C) separated by a distance of 10 μm were fabricated for each representative channel width. $I-V$ measurements were performed between pairs of contact pads A−B, B−C, and A−C, as shown in Figure 2d. The inset shows a sche-

matic of these three contact pads on the test structures. The measured resistance (from the slope of the $I-V$ curves) between the contact pads A and B can be written as $R_{AB} = R_{CA} + R_{DAB} + R_{CB}$, where R_{CA} (or R_{CB}) = contact resistance at pad A (or B) and R_{DAB} = device resistance between pads A and B. In this way, the contact resistance at pad B, R_{CB} can be written in terms of R_{AB}, R_{BC}, and R_{CA} as

$$R_{CB} = \frac{R_{AB} + R_{BC} - R_{AC}}{2} \quad (1)$$

From three different test structures for each channel width, we found that the contact resistance was within 20% of the total resistances of the test structure. These values did not change appreciably after the Pt decoration experiments described later.

Having characterized the pristine interconnect test structures, we now turn toward maximizing their electrical properties for interconnect applications. As-received SWNTs are a mixture containing approximately 2/3 semiconducting and 1/3 metallic carbon nanotubes. In aligned architectures such as ours, due to the high resistance of the semiconducting nanotubes (almost 2−3 orders of magnitude larger than that of metallic nanotubes),[20] only 1/3 of the nanotubes actively conducts current, and the rest remain dormant, vastly degrading the potential performance of the interconnect structure. Moreover, we find that our narrower lateral SWNT architectures tend to have higher resistivity, presumably due to decreased number of metallic conduction paths within the nanotube arrays. Hence, it is essential to change the electrical property of semiconducting nanotubes into metallic ones for nanoscale interconnect applications. Our past work has shown that Pt decoration of carbon nanotubes can be an effective method for increasing the number of conduction channels near the Fermi level,[16] which increases the conductance of multi-wall carbon nanotubes. Question arises if similar effects can be used to improve conductance of SWNTs, as well. To elucidate the possible underlying effects of Pt nanocluster decoration on the electronic band structure of metallic and semiconducting SWNTs, we first present *ab initio* density functional theory (DFT) calculations (see Supporting Information) on these systems. The calculations are based on a super cell approach with periodic boundary conditions, where Pt clusters lie at the center of each supercell. Detailed calculations were performed for two semiconducting SWNTs (with chiralities [8,0] and [10,0]) and one metallic ([9,0]) SWNT, for increasing number of Pt atoms (n = 0−13) per cluster. Our calculations show that the introduction of Pt atoms gives rise to new electronic bands near the Fermi level of all the SWNTs that directly impact the band gap, which defines the semiconducting or metallic nature of the nanotubes. Figure 3a shows the variation of band gap ΔE_G

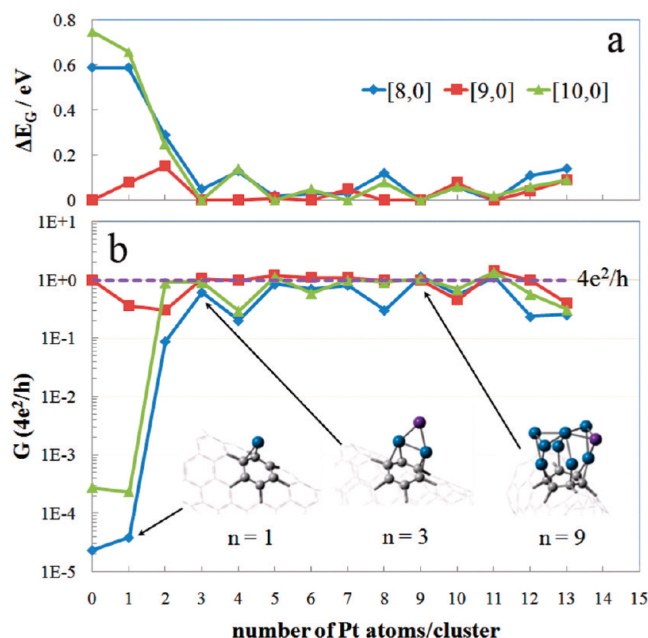

Figure 3. Calculations showing the effect of Pt decoration on electronic properties of SWNTs. (a) Band gap closing in semiconducting [8,0] and [10,0] SWNTs due to Pt nanocluster decoration. The gaps close within 3-Pt coverage and then remain close to zero. The metallic [9,0] nanotube remains metallic after 3-Pt coverage. (b) Effect of Pt decoration on the zero-bias Landauer conductance at T = 300 K in a semilog plot. The conductance of the semiconducting nanotubes [8,0] and [10,0] increases by several orders of magnitude and approach G = $4e^2/h$ within 3-Pt decoration and fluctuate close to this value. The metallic [9,0] nanotube remains metallic without any significant drop in conductance. In some cases, the conductance G in both metallic and semiconducting nanotubes exceeds $4e^2/h$. The insets show the optimized structures of representative cluster sizes. The purple atoms are the last ones to be added.

in the three SWNTs for different number of Pt atoms, n, per cluster. We see that, with increasing number of Pt atoms per cluster, the band gaps of the semiconducting nanotubes [8,0] and [10,0] rapidly approach $\Delta E_G \approx 0$ by $n = 3$ and then remain close to zero for $n > 3$. For the metallic nanotube [9,0], the gap remains very close to zero for almost all values of n. Further, the proximity of these additional bands to the Fermi level enhances their contribution to the total conductance compared to the pristine SWNTs. Figure 3b shows a semilog plot of the zero-bias Landauer conductance[21,22] as a function of the number of platinum atoms per cluster for all three SWNTs, calculated at T = 300 K. It is seen that the semiconducting nanotubes undergo 4−5 orders of magnitude increase in conductance within values of n as low as $n = 3$, approaching the value $G = 4e^2/h$. For $n > 3$, G remains orders of magnitude more conducting compared to the pristine systems and significantly close to $4e^2/h$, which makes them metallic for all practical purposes. The metallic (9,0) nanotube remains metallic. In all cases, the conductance of nanotube exceeded $4e^2/h$ for certain values of n. This indicates that uniform decoration of small (few nanometers) clusters of Pt can potentially convert semiconducting SWNTs into metallic ones

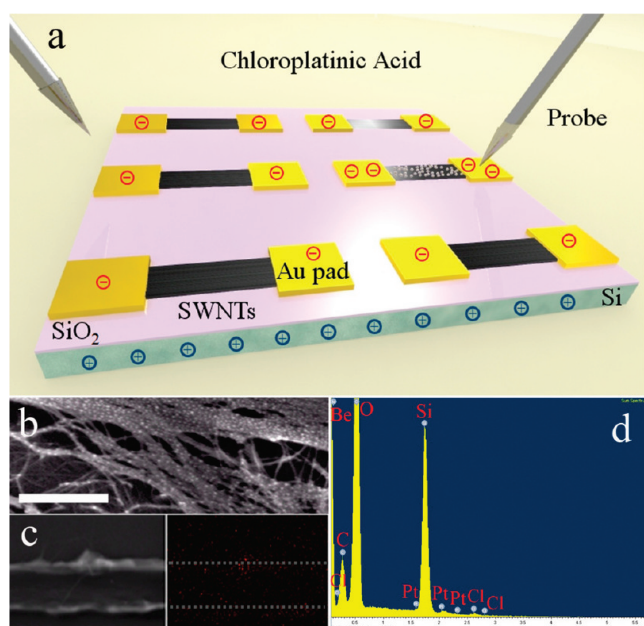

Figure 4. Pt decoration of SWNTs and its analysis using SEM and energy-dispersive X-ray spectroscopy (EDS). (a) Schematic representation of Pt decoration of SWNT test structures in a dilute chloroplatinic acid solution. The application of a negative electric potential on one of the contact pads (directly contacted) induces (indirect) negative potentials on the neighboring devices due to the capacitive effect of the oxide-coated silicon wafer. (b) Typical SEM image of Pt decoration on the surface of directly contacted SWNT bundles. Scale bar = 200 nm. (c) SEM image (left) and its corresponding EDS map (right) of indirect Pt decoration, with dashed lines indicating the position of the SWNT test structure. (d) EDS spectrum from the same structure in panel c showing that Pt nanoclusters are decorated on the SWNT belt.

and further enhance the conductance of metallic nanotubes.[23] Hence, we have adopted this procedure of Pt nanocluster decoration to improve the overall conductivity of our SWNT interconnect arrays.

Pt nanoclusters were electrochemically decorated on the SWNT arrays without disturbing their aligned architecture. Figure 4a is a schematic of the Pt decoration process on SWNTs. To decorate Pt nanoclusters on the surface of SWNTs, we immersed the assembled SWNT test structures in a 5 mM chloroplatinic acid solution. A negative potential ($-Ve$) of 50 mV was applied on a contact pad for 2 s using a Keithley 2400 sourcemeter, and the other probe was immersed in the same solution without touching any contact pads. When a negative potential is applied to the contact pad of the test structures, Pt ions having positive charges are nucleated selectively on the surface of the contact pads and the SWNT architectures. At the same time, induced negative potential is created on the neighboring test structures by a capacitive effect of the underlying highly doped Si substrate and its SiO_2 insulating layer. This resulted in decoration of smaller Pt nanoclusters (<5 nm) on the surface of the other assembled SWNT arrays, as well. We found that this "indirect" deposition was more effective as it gave clusters of extremely small size, and there was no damage to the arrays due to accidental static discharge when the probes are contacted to the pads. Figure 4b is an SEM image of SWNT arrays on which Pt nanoclusters, decorated directly, are clearly visible. Figure 4c shows an SEM image and energy-dispersive X-ray spectroscopy (EDS) map of a SWNT array indirectly decorated with Pt nanoclusters. In this case, the Pt clusters were almost indistinguishable in the SEM images, but the EDS map for Pt shows very small amounts of Pt decoration, as confirmed by the EDS spectrum in Figure 4d. The EDS map along with the spectral analysis is consistent with the fact that extremely small (~ a few nanometers) Pt nanoclusters are uniformly decorated over the surface of aligned SWNT network structures without forming a continuous Pt film. The small amount of Pt nanoclusters in the surrounding region of the SWNT array was decoration on the SiO_2 surface and did not contribute to the conducting mechanism in any way. This was confirmed by physically breaking some of the test structures after which no current was detected between the contact pads when a voltage was applied.

Figure 5a−c shows a change in resistance before and after Pt decoration for samples having widths approximately = 700, 500, and 200 nm (with five test structures for each width) and a length of 25 μm between two contact pads. The measured resistance includes the contact resistance and the device resistance. Most test structures undergo a large reduction of resistance with Pt decoration, which is consistent with our theoretical results. In the case of a 700 nm channel width, the average total resistance of pristine test structures was about 4.6 kΩ, which dropped to 3.1 kΩ after Pt decoration reducing 33% of its resistance on average. The drop in average resistance was found to be 64 and 49% in the case of 500 and 200 nm channel widths, respectively. The resistivity of test structures with different channel widths (before and after Pt decoration) is shown in Figure 5d. To calculate the resistivity, the length and width (at five positions along the length) of the test structures were obtained from SEM images, and height was averaged from 15 points on the same structure using cross-sectional AFM height measurements. We found that, as the channel widths of the SWNT arrays decrease, the values of resistivity increase, indicating a great dominance of semiconducting nanotubes in the narrower structures. The average decrease of resistivity after Pt decoration is hence also different for different channel widths. In the case of a 200 nm channel width, resistivity is reduced by 52% changing from 7.385 to 3.534 mΩ·cm. The drop in resistivity was found to be about 48 and 34% for 500 and 700 nm channel test structures, respectively, after the Pt decoration. The obtained resistivities have higher values (~1 order of magnitude) compared to reports by other groups on individual SWNT ropes.[24,25] This is a direct outcome of the fact that our "electrode on top of sample" configuration allowed the formation of contacts with only the outer nanotubes of the array. Since

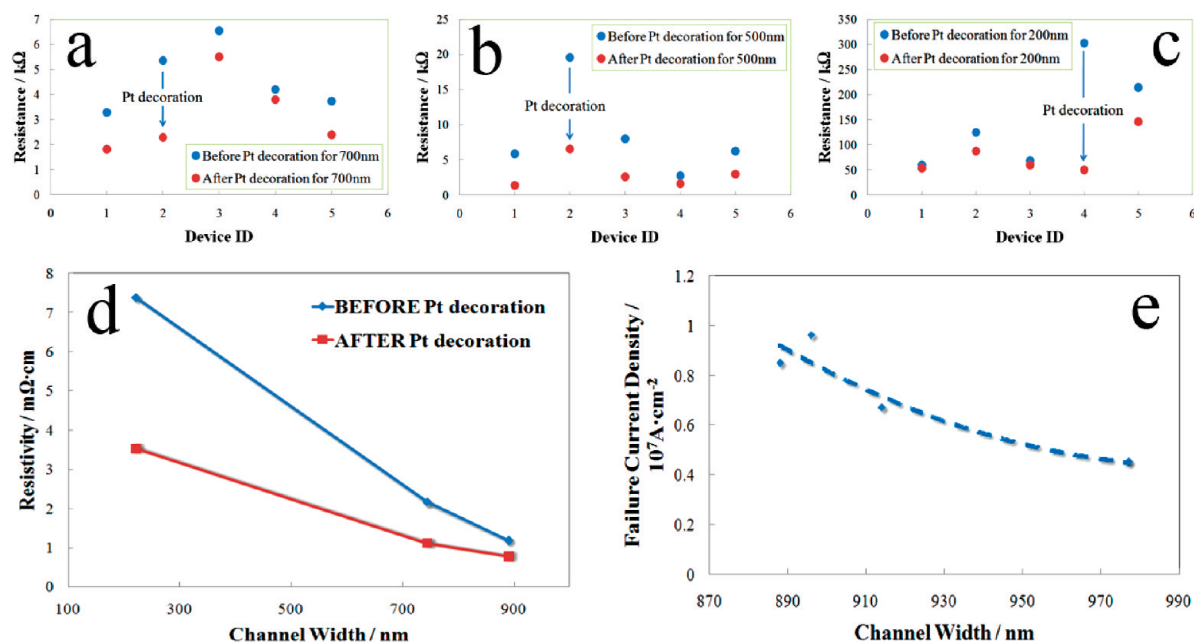

Figure 5. Electrical characterization of SWNT test structures before and after Pt decoration. (a−c) Resistance of pristine and Pt-decorated devices with 700, 500, and 200 nm channel widths. Most Pt-decorated structures exhibited dramatically reduced resistance compared to their pristine states. (d) Resistivity of structures with different channel widths before and after Pt decoration. (e) Failure current density with a guide curve for structures having various channel widths, showing that narrower devices have better current-handling capability.

inter-nanotube conductance is extremely low, most of the currents flowed through only the "contacted" nanotubes, leaving a significant portion of nanotubes dormant in the conduction mechanism (see later) but became included when the nominal resistivity was calculated using the overall geometry of the arrays. At this point, it is not possible to determine the exact number of "uncontacted" nanotubes. However, our future research will attempt to overcome this problem by fabricating arrays of extremely small heights (less than a few nanometers).

The larger percentage drop in resistivity for the narrower channels is consistent with the fact that, before Pt decoration, the overall fraction of semiconducting nanotubes between the two contacts was larger for narrower channels, which, when converted to metallic nanotubes, causes a higher percentage change. If every contacted semiconducting nanotube were to be completely converted to a metallic one *in all the test structures*, the final resistivity would be independent of channel size. From Figure 5d (where average values for five test structures have been plotted for each channel width), we find that complete "metallization" of all nanotubes in all test structures was not achieved due to variations in experimental conditions, although the slower dependence of resistivity on channel width, after Pt decoration, compared to that of the pristine structures is a very encouraging result. We will discuss this metallization issue in greater detail later.

Another important criterion for interconnect applications is the failure current density. Individual multi-walled carbon nanotubes (MWNT) can withstand current densities of $\sim10^9$ A·cm^{-2} at 300 °C for a short time.[4] Also, MWNT via structures were shown to operate at a current density of 2×10^6 A·cm^{-2}, comparable to Cu vias.[26] Individual SWNTs can withstand a current density $>10^9$ A·cm^{-2}.[27] However, it appears that such high current densities in highly organized and aligned lateral SWNT structures have not been reported so far. Failure current density was measured in our structures by increasing an applied voltage in steps of 3 V in a vacuum chamber. Figure 5e shows failure current density (the dashed line is a guide to the eye) for test structures with different channel widths. The averaged value of failure current density was 7.34×10^6 A·cm^{-2}, while the maximum failure current density was measured up to 9.62×10^6 A·cm^{-2} obtained for the narrower channels. Although these values are lower than that of individual metallic CNTs, we note that even for these calculations we have assumed that all of the nanotubes participate in the conduction of charges, whereas in reality, only a part that is electrically contacted conducts the charge carriers, hence lowering the calculated current density. In any case, the values are larger than that of MWNT via bundles and increase for lower channel widths, easily comparable to or better than that of Cu at these size scales.

Since our DFT results indicate that the Pt decoration results in the enhanced metallic behavior of semiconducting nanotubes, it is important to investigate the degree of metallization that these nanotubes in the test structures undergo. As discussed earlier, the electrode-on-top configuration does not contact all of the nanotubes electrically. Hence, from the resistivity

values itself, it is not possible to comment on how many semiconducting nanotubes were converted to metallic ones. However, since the same number of nanotubes remain in contact with the leads before and after the Pt decoration, we can use the known ratio of semiconducting to metallic nanotubes (2:1) for naturally grown SWNTs to predict the overall change in resistance if all semiconducting tubes were converted to metallic ones. We assume that this ratio is extendable to the two kinds of nanotube paths (metallic or semiconducting paths) between the two contacts of our aligned array.

Let us assume that, in any test structure, the number of nanotubes is X and the number of nanotubes electrically contacted is N, where $N < X$ (*e.g.*, N could be equal to 30% of X). Out of these N nanotubes, $N/3$ are metallic and $2N/3$ are semiconducting. In the simplest case, if we assume that the nanotubes are parallel resistors in the device, the total resistance of the pristine array of nanotubes is

$$\frac{1}{R_{\mathrm{total}}} = \sum \frac{1}{R_{\mathrm{m}}} + \sum \frac{1}{R_{\mathrm{sc}}} \tag{2}$$

where R_{m} is the resistance for a metallic SWNT and R_{sc} is resistance for a semiconducting SWNT.

To simplify calculations, let us assume that all metallic SWNTs have resistance of R_{m} and semiconducting SWNTs have resistance of R_{sc}. Then, eq 2 can be written as

$$\frac{1}{R_{\mathrm{total}}} = \sum_{n=1}^{N/3} \frac{1}{R_{\mathrm{m}}} + \sum_{n=1}^{2N/3} \frac{1}{R_{\mathrm{sc}}} \tag{3}$$

Typically, $R_{\mathrm{sc}} \gg R_{\mathrm{m}}$ by about 2−3 orders of magnitude. In this case, the term $\sum_{n=1}^{2N/3} 1/R_{\mathrm{sc}} \approx 0$ compared to the term, $\sum_{n=1}^{N/3} 1/R_{\mathrm{m}}$. Therefore, resistance of device before Pt decoration can be written as

$$R_{\mathrm{total}} = \frac{3R_{\mathrm{m}}}{N} \tag{4}$$

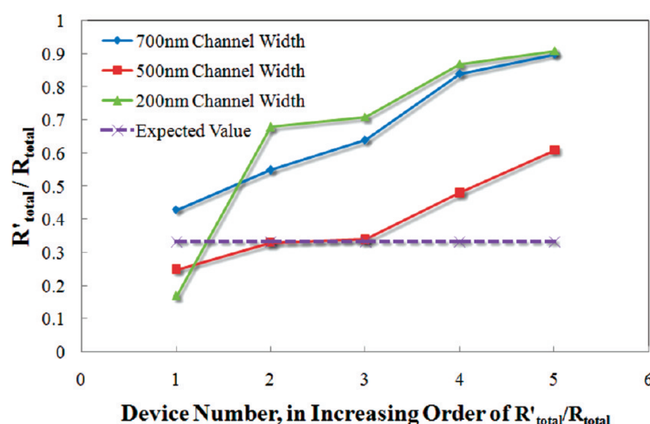

Figure 6. Comparison between predicted and experimentally measured resistance ratio of Pt-decorated and pristine test structures.

After Pt decoration, if all semiconducting SWNTs get converted to metallic ones, then their converted resistance is the same as that of the metallic SWNTs (*i.e.*, R_{m}). Therefore, the total resistance after Pt decoration would be given by

$$\frac{1}{R_{\mathrm{total}}} = \sum_{n=1}^{N/3} \frac{1}{R_{\mathrm{m}}} + \sum_{n=1}^{2N/3} \frac{1}{R_{\mathrm{m}}} = \frac{N/3}{R_{\mathrm{m}}} + \frac{2N/3}{R_{\mathrm{m}}} = \frac{N}{R_{\mathrm{m}}} \tag{5}$$

Hence, the resistance of the device after Pt decoration can be written as

$$R'_{\mathrm{total}} = \frac{R_{\mathrm{m}}}{N} \tag{6}$$

Hence, the predicted ratio of resistance between the decorated and pristine test structures

$$\frac{R'_{\mathrm{total}}}{R_{\mathrm{total}}} = \frac{R_{\mathrm{m}}/N}{3R_{\mathrm{m}}/N} = \frac{1}{3} \tag{7}$$

which is independent of how many SWNTs are electrically contacted.

Figure 6 shows the comparison between the predicted value and experimental results for the ratio of resistance before and after Pt decoration for all test structures of different channel widths. The test structures have been plotted in increasing order of the ratio values for clarity. We find that more than 25% of the devices attained the predicted ratio of 0.33 (indicating conversion to "all-metallic" test structures after Pt decoration). In the case of the other test structures, the process of Pt decoration may have been incomplete due to variabilities associated with our electrodeposition experiments in terms of time, concentration of electrolytes, electric fields, access to all nanotubes, *etc.*, and these issues will be addressed in the future. In some cases, the ratio was below 0.33, indicating that some of the metallic nanotubes may have undergone conductance enhancement, as well, as predicted by density functional theory calculations. Our future research will attempt to fabricate test structures of very low heights such that all of the nanotubes can be electrically contacted. This will remove many of the discussed ambiguities that have evolved during this work.

CONCLUSIONS

In conclusion, using a template-guided fluidic assembly process, we have fabricated highly organized, scalable, and aligned SWNT array interconnect test structures. The narrowest lateral widths of test structures presented here (∼200 nm) are limited by our current lithographic facilities and, in principle, can be reduced further down to lower sizes.

The structures become increasingly aligned with decreasing channel width. We have also demonstrated a Pt nanocluster decoration technique to enhance the overall conductive nature of these structures. Due to our top-contacted geometry that did not electrically contact all of the nanotubes, accurate estimates of resistivity of the nanotube array were not possible. However, the Pt decoration leads to significant reduction of the nominal channel resistivity, with evidence of complete conversion of the semiconducting nanotubes into metallic ones in some cases, in agreement with our calculations of band gap and Landauer conductances. These interconnect test structures are able to handle high current densities, approaching nominal values of $\sim 10^7$ $A \cdot cm^{-2}$ (comparable to or better than that of copper). The processes involved in the fabrication and performance enhancement *via* Pt decoration are simple to implement, are CMOS-compatible, and are easily scalable to wafer levels. The fabrication and performance enhancement of these interconnect test structures demonstrate a big step toward integration of carbon nanotubes into microelectronic platforms for future gigascale interconnects.

EXPERIMENTAL METHODS

The SWNT solution was obtained from Brewer Science Inc. with the mean length of 610 nm and mean diameter of 1.9 nm. The solution was composed of 0.23 wt % SWNT−DI water solution (CNTRENE C100). A silicon wafer with a 100 nm thick SiO_2 layer was obtained from the University Wafer. To improve the contact between the SWNT−deionized water solution and substrate, the substrate was pretreated using an inductively coupled plasma (ICP) with mixed gas flow of O_2 (20 sccm), SF_6 (20 sccm), and Ar (5 sccm). The substrate was then spin-coated with a PMMA film and patterned with trenches using EBL. Patterned substrate was vertically submerged into the SWNT−DI water solution using a dip-coater and gradually lifted from the solution with a constant pulling speed of 0.5 $mm \cdot min^{-1}$. Two dip-coating processes with 180° rotation were applied to make a better coverage of SWNTs along with the trenches. After this assembly process, a PMMA film was removed in acetone and rinsed in DI water. Then, the substrate was dried with nitrogen. For electrical characterization, contact pads were fabricated on the surface of SWNTs and oxide substrate using EBL and Ti (5 nm)/Au (150 nm) deposition followed by a lift-off process. To decorate Pt nanoclusters on the surface of SWNT test structures, we completely immersed them in a 5 mM chloroplatinic solution and then applied a negative electric potential (−*Ve*) of 50 mV on a contact pad with one side probe for 2 s using a Keithley 2400 sourcemeter, and another probe was located at the same solution without touching any contact pads. The electrical characterization was conducted using a Janis ST-500 electrical probe station connected to a Keithley 2400 sourcemeter.

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Supporting Information Available: Details of Raman spectroscopy for the characterization of the alignment, and details for calculation of band gap and conductance. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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